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Waveform Display for Slowly Varying Signals

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Slowly changing signals will appear on an oscilloscope as a moving dot. A circuit is described which permits such waveforms to be fully displayed in real time. The oscilloscope screen functions as a window across which the signal scrolls at a user selectable rate.

Instrumentation for the capture of fast analog signals has been the subject of numerous research publications. Typical of such contributions are the fast transient digitizer of Crosby and MacAdam[1] and the boxcar integrator of Taylor *et al.*[2]

However, in many physical measurements it is necessary to display *slowly* changing signals. Most laboratory oscilloscopes have relatively fast phosphors which will exhibit a moving dot rather than a continuous trace for signals spanning more than a fraction of a second.

The circuit presented here permits such slow waveforms to be fully displayed on any laboratory oscilloscope. In operation it is rather like an electronic strip-chart recorder in the sense that the signal will be observed to slide across the scope face at a user selectable "scroll rate" (the analog of an adjustable chart speed). As indicated in Fig. 1, the oscilloscope

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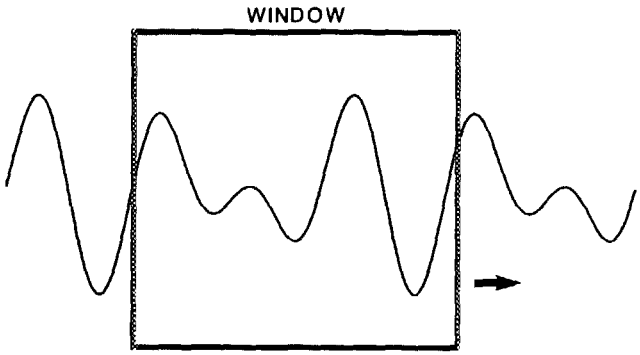

FIG. 1. Signal waveform and observation window.

screen functions as a display window which is scanned along the signal waveform.

The design provides for two input channels. A "freeze" mode is included which allows the user to instantly stop the displayed waveform.

The complete circuit is shown in Fig. 2 and the essential timing sequences are illustrated in Fig. 3. Put simply, during a time interval T_1 the waveforms stored in RAM are unloaded and displayed. At the same time, N new samples are loaded into FIFO registers (N can be 1, 2, 4, or 8 and is selected by the TTL logic inputs S_0 and S_1). During a second shorter interval T_2, the N oldest sample bytes are discarded from the memory while the N new samples in the FIFO registers are transferred into the memory. The particular manner in which this periodic replacement is performed results in the scrolling feature already mentioned.

We now discuss the circuit activity in detail. Assume MODE = 0 (RUN).

(a) *Interval* T_1: The Q output of FF1 is 0. Clock pulses are thus being passed to both counters 1 and 2. On each rising edge of the mth bit of counter 1 (where $N = 2048/2^m$), the one shot will trigger a digital conversion of the input signal. This conversion command will occur N times during T_1.

As each of the conversions is completed by the ADC0804, the $\overline{\text{INT}}$ line will go low. This sends a shift-in command to the pair of 16 by 4 bit FIFO registers. Thus the 8-bit digitized signal is shared between the two CD40105's. The $\overline{\text{INT}}$ signal also clocks FF2, which toggles, forcing the analog multiplexer to alternate between channels 1 and 2. At the end of T_1 the FIFO registers contain N 8-bit signal samples. If $N = 2,4$, or 8, then $N/2$ of these samples belong to channel 1 and $N/2$ to channel 2. When $N = 1$, only one new sample will be stored during T_1 and so two successive complete cycles are necessary to acquire data from both channels.

Concurrent with the digitizing described above, the previous contents of the 2-kbyte RAM are read out during the interval T_1. This integrated circuit contains 1024 samples of ch. 1 in its even addresses and 1024 samples of ch. 2 in its odd addresses. The total of 2048 RAM addresses are provided in sequence by counter 2 with the contents of alternate memory locations being sent to each of the two D/A converters which drive the oscilloscope inputs.

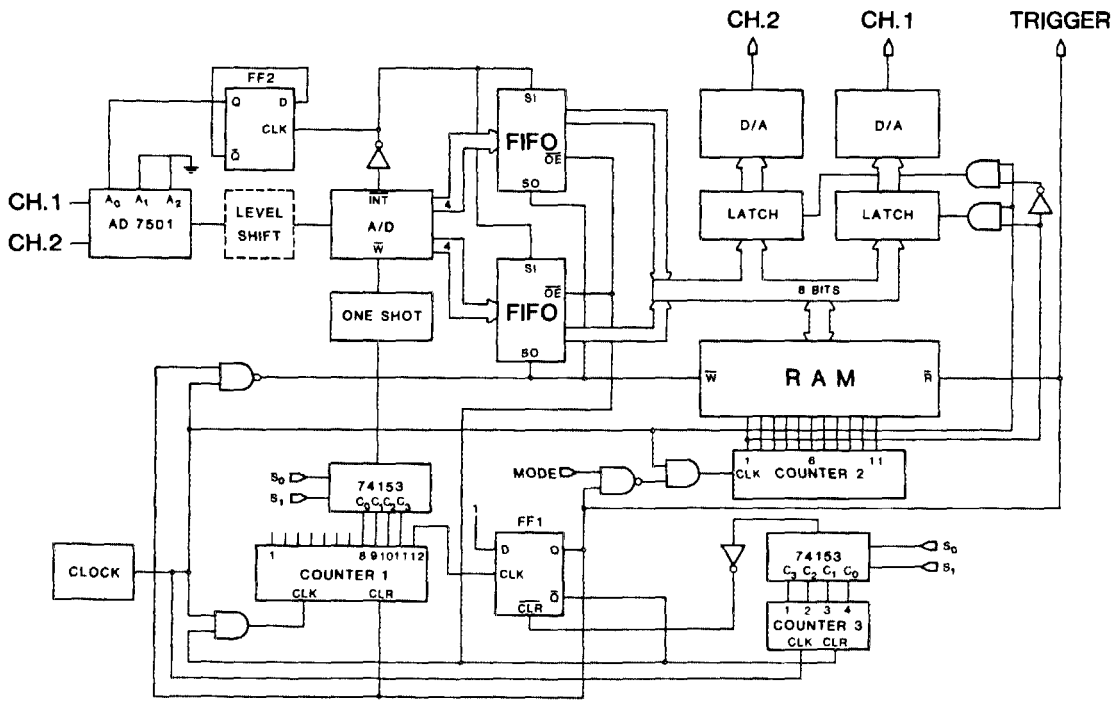

FIG. 2. Waveform display circuit. This schematic is slightly simplified and does not include external reset logic. S_0 and S_1 are TTL inputs for scroll rate selection. Level shifting is required if the input signal lies outside the range specified for the A/D converter. Counters 1 and 2 are each made up of three 74393 binary counters. The RAM is a Toshiba TMM 2016, or equivalent. Other components are as follows. Flip–flops: 7474; one-shot: 74123; A/D: Intersil ADC 0804; D/A: National Semiconductor DAC 0800; FIFO: RCA CD40105; Latches: 74273.

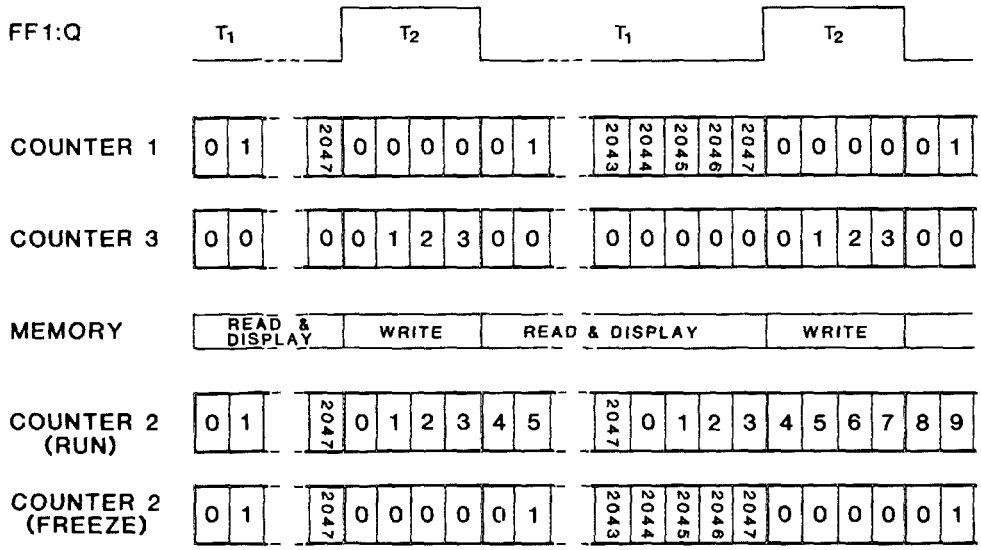

FIG. 3. Count sequences during the RAM transfer-in and transfer-out intervals for $N = 4$.

(b) *Interval* T_2: The clock pulse following T_1 will trigger FF1 via bit 12 on counter 1. This immediately resets counter 1, enables counter 3, and sets the RAM to the WRITE mode. For the interval T_2, Q of FF1 remains high, thus preventing clock pulses from reaching counter 1. Counter 2, however, begins a new sequence 0–2047, as shown in Fig. 3. During T_2 the FIFO tri-state outputs are enabled via $\bar{Q}$ of FF1. The N clock pulses which reach the shift-out pins of the FIFO's cause the previously stored samples to be transferred to the RAM addresses generated by counter 2. The interval T_2 is terminated when the nth bit (where $2^{n-1} = N$) of counter 3 briefly goes to 1 thus clearing FF1 and counter 3, and enabling counter 1.

As can be seen in Fig. 3, during the second T_1 interval, counters 1 and 2 are skewed relative to one another. This causes the display to begin at memory address N, continue through 2047 and then pick up addresses 0 to $N-1$. The third T_1 interval begins with address $2N$, counts to 2047, and continues from 0 to $2N-1$. In other words, in each cycle $N/2$ old samples per channel are discarded and $N/2$ new samples per channel are added to the end of the display. As remarked earlier, the case $N = 1$ is slightly different, with only one of the channels being updated per cycle. Notice that in the FREEZE mode (MODE = 1) counter 2 is inhibited during T_2 and so remains in phase with counter 1.

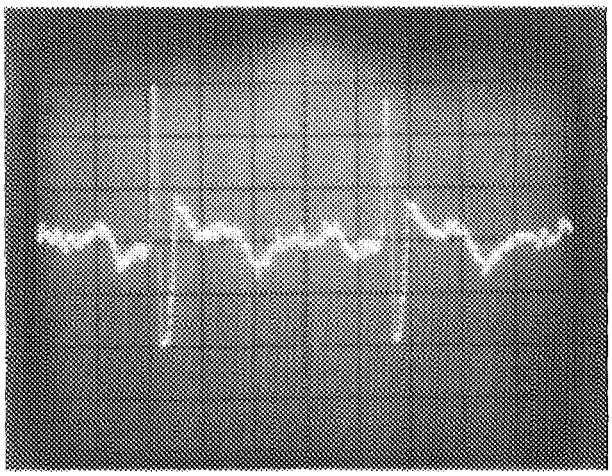

FIG. 4. ECG waveform displayed in the FREEZE mode. The total width of the record is 4.1 ms.

With a 500-kHz system clock, the display window width T_1 is 4.1 ms. The maximum scrolling rate will occur when $N = 8$. In this case the time required for the display to scroll one complete frame is 1.05 s. The slowest scrolling occurs for $N = 1$ and is 8.4 s per frame. Larger values of T_1 and correspondingly slower scroll rates may be obtained by choosing a system clock of lower frequency.

The maximum conversion rate demanded of the A/D is determined by the case where eight new samples are taken during T_1; each 8-bit A-to-D conversion must then be completed within 512 μs. The digital-to-analog converters operate at a constant rate of 1024 points/channel during T_1. Hence, the D to A conversion time must be less than 4 μs.

Although it is not shown in the schematic (Fig. 2), the circuit also has the added capability to transfer RAM contents to a personal computer for subsequent processing and analysis. This operation is performed in the FREEZE mode and takes place via an RS232 port designed around a standard UART chip.

The waveform display was designed as a general purpose laboratory instrument. We anticipate that it will prove to be a useful addition to experimental studies of phenomena which typically exhibit relatively slow time-dependent signals. This includes, for example, thermal, acoustic, and photoconductive effects.

We have utilized the circuit to provide a real-time display of electrocardiogram waveforms. The apparatus consisted of a Phipps and Bird Lead Selector and a Phipps and Bird Model 631 preamplifier. The waveform shown in Fig. 4 was obtained by feeding the left arm–right arm differential voltage (from the modules mentioned above) through an additional stage of amplification and then to the display unit. The oscilloscope was a Tektronix 2215, and was set on Ex-

ternal Trigger with a time base of 0.5 ms/cm. The photograph was taken after the circuit was switched to the FREEZE mode.

The ECG pulses clearly contain the low-amplitude, high-frequency component known as muscle artifact, as well as the general features characteristic of such biomedical signals.

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